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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,141	08/29/2005	Giovanni Tricomi	1001/0166PUS1	5064

60601 7590 07/29/2010

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ART UNIT	PAPER NUMBER
2892	

MAIL DATE	DELIVERY MODE
07/29/2010	PAPER

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/531,141
Filing Date: August 29, 2005
Appellant(s): TRICOMI ET AL.

Patrick J. O'Shea
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 24 May 2010 appealing from the Office action mailed 24 November 2009.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

(6) Grounds of Rejection to be Reviewed on Appeal

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner. Claims 22 and 23 were rejected under 35 USC 112, first paragraph, as failing to comply with the written description requirement. Upon further review, the Examiner recognizes the discloses in paragraph [0007] of the specification to support the claim to "a of at least one of the stamped pedestals is between 1/10 of a height of the carrier device to a height of the carrier

device", as recited in claim 22, and similarly in claim 23. Although paragraph [0007] of the specification recites the height of the pedestals to be from about 1/10 of the material thickness of the carrier to the carrier thickness itself, one of ordinary skill in the art would recognize the interchangeability between the words "thickness" and "height'. Therefore, the rejection of claims 22 and 23 under 35 USC 112, first paragraph, is withdrawn.

The appellant's statement of the grounds of rejection with respect to independent claims 16 and 17, and dependent claims 2 - 8, 13 - 15, and 22 - 25, under 35 USC 103(a) to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 2 – 7, 13, 14, 16, 17, and 22 - 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pritchard et al. (US 5,479,050, prior art of record) in view of Kwon et al. (US 5,365,409, prior art of record).

a. Regarding claim 16, **Prichard discloses an integrated circuit** (e.g. figure 1), **comprising:**

a semiconductor die (die 11);

a carrier device comprising a die paddle onto which the die is attached (paddle 16, disclosed in col. 1, line 65, which is the portion of leadframe 10 under semiconductor die 11), **where a plurality of stamped pedestals** (pedestals 12 and 13, disclose in col. 1, lines 65 – 67 to be stamped) **are arranged on the carrier device exteriorly surrounding and adjacent to the die paddle** (e.g. as seen in figure 1, the pedestals 12 and 13 exteriorly surround and are adjacent to the top of the die paddle region under the semiconductor die 11), **where the carrier device, the die paddle and the stamped pedestals form a single piece unitary structure** (e.g. as seen in the figure, the carrier device, die paddle, and stamped pedestals are formed from a single piece);

a plurality of leads (leads 17 and 18) **each comprising an inner lead portion** (inner portion towards the die) **that extends to an outer lead portion** (outer portion furthest away from the die); **and**

a first bond wire extending from the die to a first of the plurality of stamped pedestals (bond wire 15)**, and a second bond wire extending to an inner lead portion** (bond wire 22).

Pritchard is silent with respect to explicitly disclosing that the plurality of leads are metallic, the second bond wire extends from the first of the plurality of stamped pedestals to the inner lead portion, and a

package that encapsulates the semiconductor die, the die paddle, the first and second bond wires and the inner lead portions.

Kwon discloses an integrated circuit structure (e.g. figure 5), **comprising a first bond wire** (bond wire 160) **extending from the die** (die 154) **to a first of the plurality of pedestals** (pedestals 158), **and a second bond wire** (bond wire 162) **extending from the first of the plurality of pedestals to an inner lead portion** (inner lead portion of lead 156); **and a package that encapsulates the semiconductor die, the die paddle, the first and second bond wires and the inner lead portions** (e.g. as seen in figure 5, there is a package, denoted by a dashed line, that encapsulates the die, paddle, wires and inner lead portions).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that the second bond wire extends from the stamped pedestal to the inner lead portion since Pritchard discloses that electrical connections may be formed between the die, pedestals, and surrounding leads, and Kwon discloses that connections between pedestals and surround leads can be made. One would have been motivated to form a wire bond between the semiconductor die and the pedestal, and between the pedestal and the inner portion of the lead in order to relieve the wire bond of stress formed by making a direct connection between the semiconductor die and the inner portion of the lead.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that a package encapsulates the die, die paddle, inner lead portions, and bond wires since it was well known in the art that semiconductor structures are encapsulated in such a manner, as supported by Kwon. One would have been motivated to encapsulate the structure in order to protect the inner device elements from external stresses.

Furthermore, although Pritchard does not explicitly disclose forming the surrounding leads from metal, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that the surrounding leads were formed from metal since Pritchard discloses connecting the leads to the die via wire bonds to form an electrical circuit, and it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See MPEP 2144.07. One would have been motivated to use metal for the surrounding leads since it is electrically conductive, durable, and inexpensive.

b. Regarding claim 17, **Pritchard discloses an integrated circuit** (e.g. figure 1), **comprising:**

a semiconductor die (die 11);

a carrier device comprising a planar surface onto which the die is attached (paddle 16, disclosed in col. 1, line 65, which is the portion of leadframe 10 under semiconductor die 11), **where a plurality of stamped**

pedestals (pedestals 12 and 13, disclose in col. 1, lines 65 – 67 to be stamped) **are arranged on the carrier device exteriorly surrounding and adjacent to the planar surface** (e.g. as seen in figure 1, the pedestals 12 and 13 exteriorly surround and are adjacent to the top of the die paddle region under the semiconductor die 11), **where the carrier device, the die paddle and the stamped pedestals form a single piece unitary structure** (e.g. as seen in the figure, the carrier device, die paddle, and stamped pedestals are formed from a single piece);

a plurality of leads (leads 17 and 18) **each comprising an inner lead portion** (inner portion towards the die) **that extends to an outer lead portion** outer portion furthest away from the die); **and**

a first bond wire extending from the die to a first of the plurality of stamped pedestals (bond wire 15)**, and a second bond wire extending to an inner lead portion** (bond wire 22).

Pritchard is silent with respect to explicitly stating that the carrier device and the plurality of leads are "metallic", and the second bond wire extends from the first of the plurality of stamped pedestals to the inner lead portion.

Kwon discloses an integrated circuit structure (e.g. figure 5), **comprising a first bond wire** (bond wire 160) **extending from the die** (die 154) **to a first of the plurality of pedestals** (pedestals 158), **and a second bond**

wire (bond wire 162) **extending from the first of the plurality of pedestals to an inner lead portion** (inner lead portion of lead 156).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that the second bond wire extends from the stamped pedestal to the inner lead portion since Pritchard discloses that electrical connections may be formed between the die, pedestals, and surrounding leads, and Kwon discloses that connections between pedestals and surround leads can be made. One would have been motivated to form a wire bond between the semiconductor die and the pedestal, and between the pedestal and the inner portion of the lead in order to relieve the wire bond of stress formed by making a direct connection between the semiconductor die and the inner portion of the lead.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to use a metallic material in the carrier device of Pritchard, since Pritchard discloses connecting leads to the carrier device (stamped pedestals) to form an electrical circuit, and it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshin*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945). One would have been motivated to make the carrier device metallic in order to create a conductive portion of the carrier to complete an electrical circuit, as well as allowing the pedestals to be formed easily by stamping.

Furthermore, although Pritchard does not explicitly disclose forming the surrounding leads from metal, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that the surrounding leads were formed from metal since Pritchard discloses connecting the leads to the die via wire bonds to form an electrical circuit, and it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See MPEP 2144.07. One would have been motivated to use metal for the surrounding leads since it is electrically conductive, durable, and inexpensive.

c. Regarding claim 2, **Pritchard in view of Kwon disclose the integrated circuit of claim 16, as cited above, wherein the stamped pedestals have sidewalls with an angle (α) greater than 45 degrees with respect to a plane of the carrier device die paddle** (e.g. figures 1 and 3 of Pritchard show the angle of the pedestal sidewall has an angle of 90 (figure 1) and greater than 45 degrees (figure 3) with respect to the top or bottom plane of the die paddle).

d. Regarding claim 3, **Pritchard in view of Kwon disclose the integrated circuit of claim 16, as cited above, wherein the stamped pedestals each have a plane surface which is parallel to a chip connection area plane of the carrier device** (e.g. as seen in figure 3 of Pritchard) **and each has an area for connection of a single bonding wire** (e.g. as seen in figure 1 of Pritchard,

there is an area surrounding the bond wire connection on the pedestals 12 and 13 for connecting a single bond wire 14 or 15).

e. Regarding claim 4, **Pritchard in view of Kwon disclose the integrated circuit of claim 16, as cited above, wherein a height of each of the stamped pedestals lies in the range between 1/10 and 1.5 times the height of the semiconductor die** (as seen in figure 3 and disclosed in col. 2, lines 15 - 17 of Pritchard, the stamped pedestals have a height the same as the semiconductor die, and therefore are within the claimed range).

f. Regarding claim 5, **Pritchard in view of Kwon disclose the integrated circuit of claim 16, as cited above, but is silent with respect to a height of each of the raised pedestals lies in the range from 1/5 to twice a material thickness (h) of the carrier device. Pritchard and Kwon show that the height of the pedestal may be about 0.5 times the height of the carrier device, but it is not explicitly stated.**

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that the pedestals are within the range of 1/10 to 2 times the height of the carrier device, since Pritchard and Kwon suggests through the figure this may be the case, and it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves

only ordinary skill in the art. *In re Aller*, 105 USPQ 233. One would have been motivated to make the height of the pedestal within the range of the carrier device in order to reduce lead length and stress on the leads.

g. Regarding claims 6 and 7, **Kwon discloses the structural limitations of the integrated circuit, as cited in claim 16. The process by which the raised pedestal is formed is not given patentable weight since the patentability of a product does not depend on the method of production. See MPEP 2113.**

h. Regarding claim 13, **Pritchard in view of Kwon discloses the integrated circuit of claim 17, as cited above, where the stamped pedestals make an angle (α) greater than 45 degrees with the plane of the carrier device at all sidewalls** (e.g. figures 1 and 3 of Pritchard show the angle of the pedestal sidewalls have an angle of 90 (figure 1) and greater than 45 degrees (figure 3) with respect to the top or bottom plane of the die paddle).

Pritchard and Kwon are silent with respect to explicitly stating the sides have rounded junctions parallel to the plane of the carrier device or being rounded as a whole.

However, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that the sides of the pedestals to have rounded junctions parallel to the plane of the carrier device or are rounded as a whole, since it has been held

by the courts that a change in shape or configuration, without any criticality, is nothing more than one of numerous shapes that one of ordinary skill in the art will find obvious to provide based on the suitability for the intended final application. See *In re Dailey*, 149 USPQ 47 (CCPA 1976). It appears that the disclosed device of Kwon would perform equally well shaped as disclosed by the Applicant. One would have been motivated to have rounded pedestals since materials deposited often have rounded edges due to the formation process.

i. Regarding claim 14, **Pritchard in view of Kwon disclose the integrated circuit of claim 17, as cited above, where the height of the stamped pedestals lies in the range between 1/10 of the die height and the die height itself** (as seen in figure 3 and disclosed in col. 2, lines 15 - 17 of Pritchard, the stamped pedestals have a height the same as the semiconductor die).

j. Regarding claims 22 and 23, **Pritchard in view of Kwon disclose the integrated circuit of claims 16 and 17, as cited above respectively, where a height of at least one of the stamped pedestals is between 1/10 of a height of the metallic carrier device to the height of the metallic carrier device** (e.g. as seen in figure 3 of Pritchard, the intersection of the stamped pedestals 23 with the die pad 21 has a height between 1/10 the height of the carrier device 16 and the height of the carrier device. Furthermore, it has been held that when the prior art discloses the general conditions of the claimed invention, discovering the

optimum or workable ranges involves only ordinary skill in the art. See MPEP 2144.05).

k. Regarding claims 24 and 25, **Pritchard in view of Kwon disclose the integrated circuit of claims 16 and 17, as cited above respectively, where the metallic leads are separate from the metallic carrier device** (e.g. as seen in figure 1 of Pritchard, the leads 17 and 18 are separate from the carrier device 16) .

4. Claims 8 and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Pritchard in view of Kwon, and in further view of Carter, Jr. et al. (US 6,365,976 B1, prior art of record).

a. Regarding claim 8, **Pritchard in view of Kwon disclose the integrated circuit of claim 16, but are silent with respect to a silver or gold finish applied to the stamped pedestals.**

Carter discloses that gold or silver finishes may be applied to raised pedestals in integrated circuits (Col. 5, lines 18 - 22, disclose that the surface of the pedestals have a foil on them which may consist of silver or gold, or the pedestal may be covered with a tin-silver layer).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that there is a gold or silver finish on the raised pedestals since it was known in

the art that such pedestals in integrated circuits my have a finish applied to them, as disclosed by Carter. One would have been motivated to have a gold or silver finish applied to the pedestals since gold and silver promote the bonding of the wires to the pedestals and are highly conductive.

b. Regarding claim 15, **Pritchard in view of Kwon disclose an integrated circuit, but are silent with respect to only in the areas of the stamped pedestals, a finish, particularly silver or gold, is provided for bondability.**

Carter discloses that areas of pedestals may be provided with a gold or silver finish (col. 5, lines 20 - 22, discloses that the pedestal ("dimple") may covered with a layer of tin-silver).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that there is a gold or silver finish on the raised pedestals since it was known in the art that such pedestals in integrated circuits my have a finish applied to them, as disclosed by Carter. One would have been motivated to have a gold or silver finish applied to the pedestals since gold and silver promote the bonding of the wires to the pedestals and are highly conductive.

(10) Response to Argument

Appellants argue that the prior art of Pritchard et al. (US 5,4798,050) teaches away from connecting the pedestals (e.g. figure 1, pedestals 12a and 13a, or figure 2,

pedestals 23 and 25) to the surrounding leads (e.g. figure 1, leads 17 and 18 or figure 2, leads 27), citing that "*doing so would necessitate the use of bond wires of substantially greater length than bond wires 14, 15...and bond wires 20, 22...*" and that "*The use of longer bond wires to connect the pedestals to the leads would inevitably increase the likelihood of sagging of bond wires and destruction of the bond during temperature cycling and thermal shock*" (pages 14 - 15 of Appeal Brief). Appellants state that the prior art of Pritchard teaches a single structural connection between the grounding wires 14,15 and the leads via a bonding pad 21, which will prevent such fracturing and sag of the wires during temperature cycling and thermal shock (Pritchard, col. 1, lines 13 – 33 and lines 35 – 45) (page 13 of Appeal Brief), and therefore Pritchard teaches away from connecting the pedestals to the leads. The Examiner has relied upon teachings of Kwon et al. (US 5,365,409) to render obvious the bond wire connection of the pedestals of Pritchard to the surrounding leads of Pritchard, and maintains that Pritchard does not teach away from connecting leads from the pedestals to the surrounding leads.

Pritchard discloses that the wires connecting the semiconductor die to the raised pedestal are done such that the wires "*will not sag and contact the die in an undesirable location*" (col. 2, lines 17 - 18). This statement does NOT preclude the connection of the pedestals to the surrounding leads by a wire bond. Rather, Pritchard shows that there indeed may be wire bonds directly connected to the surrounding leads (figure 1, wire bonds 22). Although Pritchard discloses the ground bond being in an area of high stress, and the need to prevent it from sagging (co. 1, lines 18 - 24), Pritchard does not disclose or suggest that a wire bond cannot or should not be formed between the

pedestal and the surrounding leads. Pritchard merely states the concern of the ground bond connection, and the device disclosed is to help alleviate the problems associated with a larger die and a direct connection between the semiconductor die and die pad (col. 1, lines 16 - 18).

Kwon is used to teach (e.g. figures 4 and 5) that instead of a direct connection from the semiconductor die to the surrounding leads, a connection may be made between the die and a pedestal, and then from a pedestal to a surrounding lead (e.g. as seen in figure 5, wire 160 connects from the die 154 to the pedestal 158, and then wire 162 connects from the pedestal to the surrounding lead 156). Although the Appellants contend that such a connection would yield a longer bond wire, and therefore subject it more likelihood of failure (pg. 15 of Appeal Brief), the Examiner respectfully disagrees. The Examiner submits that the opposite will be the case, and that such a modification will yield a shorter bond wire, since it can be seen clearly in figure 5 of Kwon that if pedestal 158 is removed, then there will be a longer bond wire that will be needed to extend from the die 154 to the lead 156. Therefore, *the inclusion of the pedestal between the semiconductor die and the surrounding leads reduces the overall length of the bond wire*. Hence, the Examiner contends that it would indeed be beneficial to modify Pritchard to connect a bond wire from the semiconductor die to the pedestal, and then connect a bond wire from the pedestal to the surrounding lead in order to *shorten* the bond wires, not lengthen them, as argued by the Appellants, and thereby reduce the stress on the bond wires.

Furthermore, the prior art of Pritchard discloses in figure 2 that the semiconductor die 33 is surrounded by multiple leads 27, as well as pedestals 23 and 25, and that it would have been obvious to one of ordinary skill in the art to modify the structure of Pritchard such that there are bond wires between the pedestals and the surrounding leads, since Kwon also discloses a semiconductor die surrounded by multiple leads and pedestals, whereby bond wires are connected between the semiconductor die and the pedestals, and between the pedestals and the surrounding leads, for at least the purpose of reducing stress on the bond wire connections. Although the Appellants indicate that such a connection may be redundant within the device of Pritchard (page 13 of Appeal Brief), one of ordinary skill in the art would recognize that connections between several leads and the semiconductor die within a circuit may be made redundantly in order to enhance the connectivity of the device structure to various differing external devices and equipment.

The Appellants also argue that Kwon teaches away from electrically interconnecting the pedestals since the Appellants assert "*Kwon teaches using the bonding wires to connect the electrically insulated (i.e. non-electrically connected) traces/interposers 110/158 and bonding figures 156 (Kwon, col. 5, line 57 to col. 6, line 50)*" (page 14 of Appeal Brief). However, the Examiner notes that Kwon clearly discloses the traces/interposers 110/158 to be conductive in col. 6, lines 11 – 12 and col. 6, line 57. Therefore, clearly Kwon teaches the pedestals 110/158 to be electrically

connected to the semiconductor die 154 and the surrounding leads 106/156 by bond wires 160/162 and 116/124.

The Appellants also state that because the substrate of Kwon is electrically insulating, that the Kwon teaches away from electrically connecting the pedestals to the semiconductor die and surrounding leads (e.g. pages 14 and 16 of Appeal Brief). The Examiner submits that the properties of the substrate are not germane to the teaching relied upon for the combination of Kwon with Pritchard. Instead, the Examiner has used Kwon to teach the formation of multiple leads and pedestals surrounding a semiconductor die, and the interconnection of the leads via wire bonds and pedestals (as seen in figures 4 and 5 of Kwon). Hence, it is the connection of the leads to the pedestals of Kwon that is used to modify the device of Pritchard, and not the material of the substrate. Although the Appellants argue that there is no reason to ground the substrate of Kwon (pg. 16 of Appeal Brief) by connecting it in the manner disclosed by Pritchard, the Examiner submits that the Pritchard is being modified to use the bond wire connections between pedestals and surrounding leads, as shown in figures 4 and 5 of Kwon, and not to necessarily connect the pedestals to the substrate of either Kwon or Pritchard. One of ordinary skill in the art would recognize that connections between several leads and the semiconductor die within a circuit may be made in order to enhance the connectivity of the device structure to various differing external devices and equipment, whereby the use of pedestals would be advantageous to reduce the bond wire length between the semiconductor die and surrounding leads, thereby reducing stress on the bond wires.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Robert Huber/

Examiner, Art Unit 2892

Conferees:

/Thao X Le/

Supervisory Patent Examiner, Art Unit 2892

/Michael J Sherry/

Quality Assurance Specialist, TC 2800